400G: Looking Forward to 800G and Terabit Speeds

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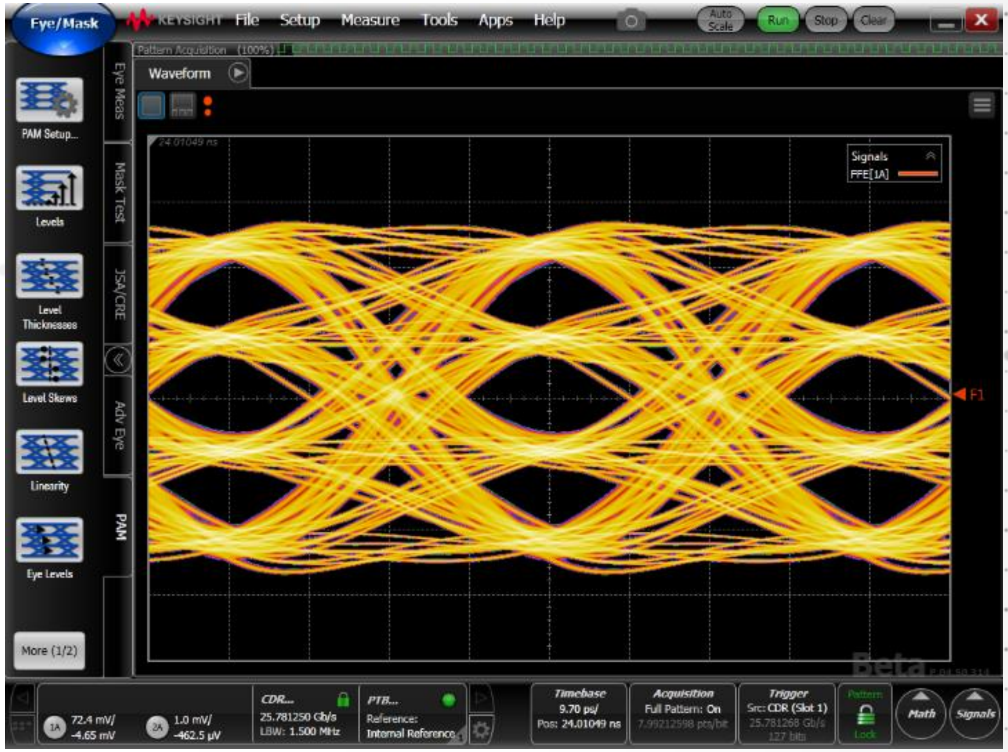
Internet Infrastructure Solutions / Keysight Technologies

Agenda

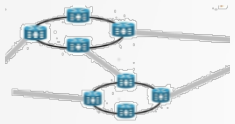
- 400G Technologies – Landscape
  - Why PAM4
  - Status of today's 400G/800G Standards?
- PAM4 - From Simulation to Measurements
- 400G → 800G Measurements
  - PAM4 Device Characterization
  - Direct Detect Output (Transmitter) Test
  - Coherent Optical Test
  - Layer 2-3 Analysis
- Summary



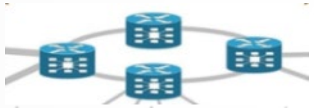
Wireline Internet Infrastructure

Core Network

Data Center

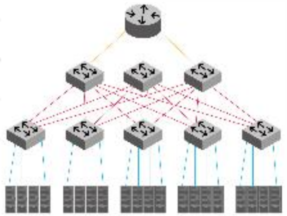


Longhaul/ undersea



Metro-Telecom

DCI



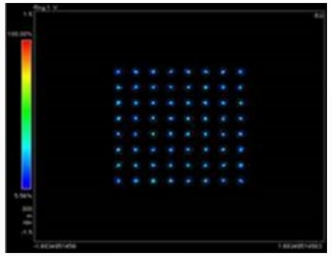
Intra-DC

Network

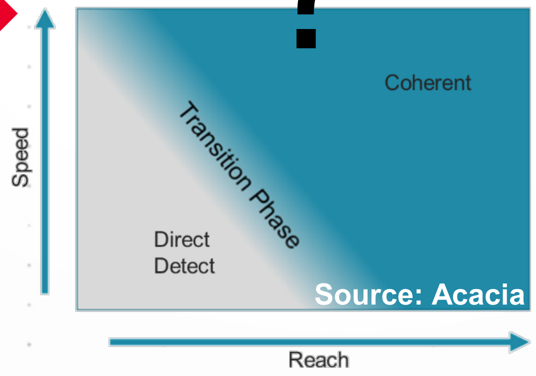
Server

100 km – 39,000 km 60 mi – 24,000 mi	10 km – 100 km 6 mi – 60 mi	10 km – 40 km 6 mi – 25 mi	20 m – 10 km 22 yd – 6 mi	1 mm – 3 m .04 in – 10 ft

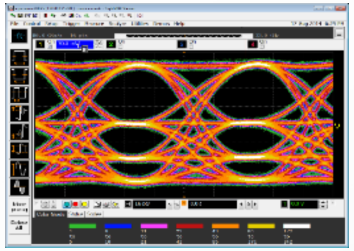
Coherent
How low can you go - still being affordable?

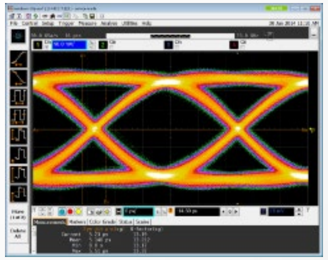


?



NRZ / PAM4
How far can you go without compromising signal quality?

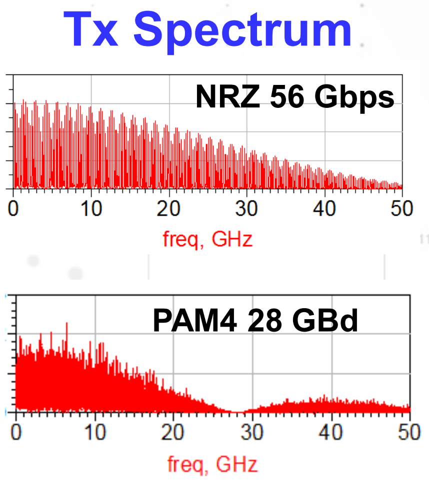




Why Does the Industry use PAM4?

ENABLES HIGHER DATA THROUGHPUT

- NRZ > 28 Gb/s limits trace length or increases cost due to more expensive PCB material
- PAM4 yields 2 bits / symbol
  - ✓ Effectively halves the channel BW needs
- Enables designers to develop products that meet the cost structure and are based on mature 100G optical components.



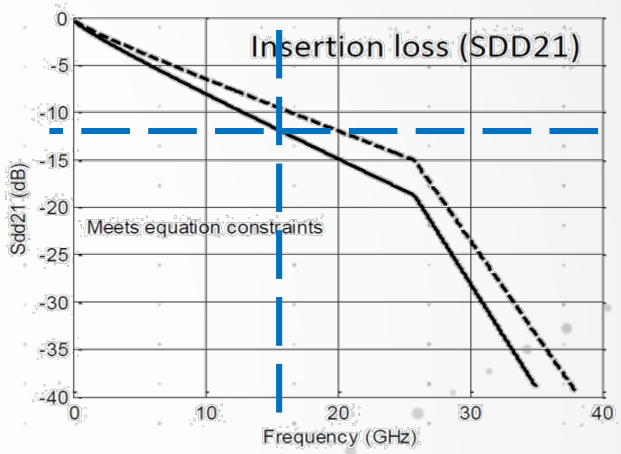
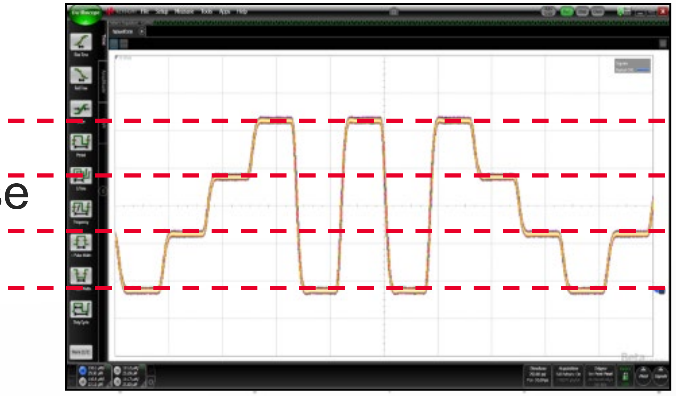
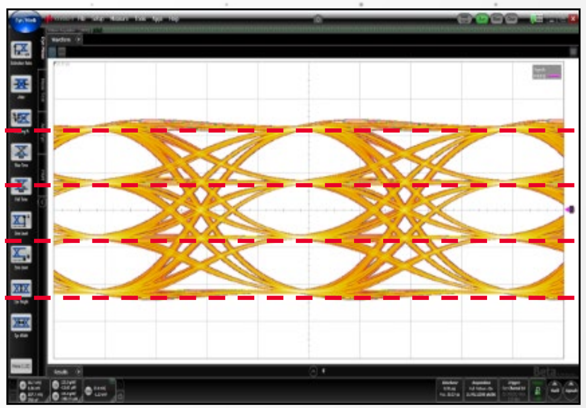


Figure 5: CEI-56G VSR NRZ channel

+ PAM4: Pulse Amplitude Modulation 4-level
+ 2 bits of information in every symbol
  - ✓ ~ 2x throughput for the same baud rate
  - ✓ 26.56 GBd PAM4 = 53.125 Gb/s
- Higher SNR requirement, more susceptible to noise → 3 eyes vs. 1 eye → **FEC essential**
- More complex PHY Chip design, linear TIA and RF driver Amp





State of the ‘400G Class’ Standards

CURRENT GENERATION - 50G LANE RATE

Direct Detection

	Standard	Description	Status
✓	OIF-CEI-56G	5 reaches, PAM4 up to 29 GBd, NRZ up to 58 Gb/s	Released
✓	IEEE 802.3bs 200/400G (Ethernet)	Medium reach SMF + C2C, C2M, PAM4 @ 53.1 & 26.6 GBd	Released
✓	IEEE 802.3cd: 50/100/200G (Ethernet)	Short reach MMF + C2C, C2M, backplanes & cables, PAM4 @ 26.6 GBd	Released
✓	64G Fibre Channel	100 m - 2 km reaches in MMF & SMF, PAM4 @ 28.9 GBd	Complete, pending publication
✓	100G Lambda MSA Group	2 m >= 2 km in SMF, 8 x 53.125 Gb/s or 4 x 106.25 Gbps PAM4	Released
	IEEE 802.3cm 400G	Short reach in MMF, PAM4 @ 26.6 GBd	Under development
	IEEE 802.3cn 50/100/200/400G	>10 km SMF (target 40 km), PAM4	Under development

Coherent Detection

	Standard	Description	Status
	OIF 400ZR	80 - 120 km SMF, DP-16QAM @ 60 GBd, coherent	pending
	IEEE 802.3ct 100/400GBaseZR	80 - 120 km SMF, DP-16QAM, coherent, (based on OIF 400ZR)	Under development

* COBO (Consortium for On-Board Optics)

Next-Generation ‘800G Class’ Standards

112G LANE RATES

Standard	Description	Status
OIF CEI-112G	5 reaches PAM4, CNRZ-5 * mainly C2C	Project starts for 5 reaches, C2M at 5th draft
IEEE 802.3ck	C2M & C2C for 2nd wave 400GbE & 800G	First baseline draft for C2M, May 2019 (based on OIF CEI-112G-VSR, MR, and LR)
Fibre Channel PI-8 128GFC	Moving closer to Ethernet baud rate	Project Start

* CNRZ-5: Chord Signaling NRZ-5 --> 5 bits transferred over 6 wires

Is 800G Really Starting Yet?

- First equipment using 400G is close to deployment
- Few remaining initial wave of ‘400G class’ standards finishing up
- **No** 802.3 official study groups started for first 800G optical links yet, will follow electrical groups
- Electrical chip-to-module, chip-to-chip, and backplane interface projects have started supporting >112 Gb/s per lane

400G Solution Overview

END-TO-END SOLUTIONS FROM KEYSIGHT FOR DIRECT DETECTION

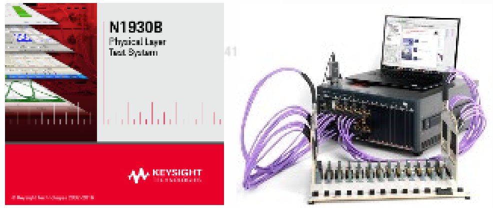
ixia
A Keysight Business

ARESONE-400GE

L2/L3 400GE Protocol Test

Modeling / Link Simulation

ADS, FlexDCA link



PLTS + M980Xa VNA

Channel/ Interconnect

400G
Design
Cycle

M8040A BERT

M8194A AWG
120 GSa/s

Receiver

UXR Scope Family
4ch, 110 GHz, 256 GSa/s
Real-Time Scope

N1000A DCA-X /
N1092A DCA-M
Sampling Scope

Transmitter

800G Solution Overview

END-TO-END SOLUTIONS FROM KEYSIGHT FOR DIRECT DETECTION

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A Keysight Business

tbd by IEEE

L2/L3 800GE Protocol Test

Modeling / Link Simulation

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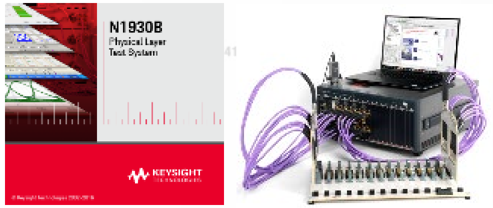
800G Design Cycle



PLTS + M980Xa VNA

Channel/ Interconnect

M8040A BERT

M8194A AWG
120 GSa/s

Receiver

UXR Scope Family
4ch, 110 GHz, 256 GSa/s
Real-Time Scope

N1000A DCA-X /
N1092A DCA-M
Sampling Scope

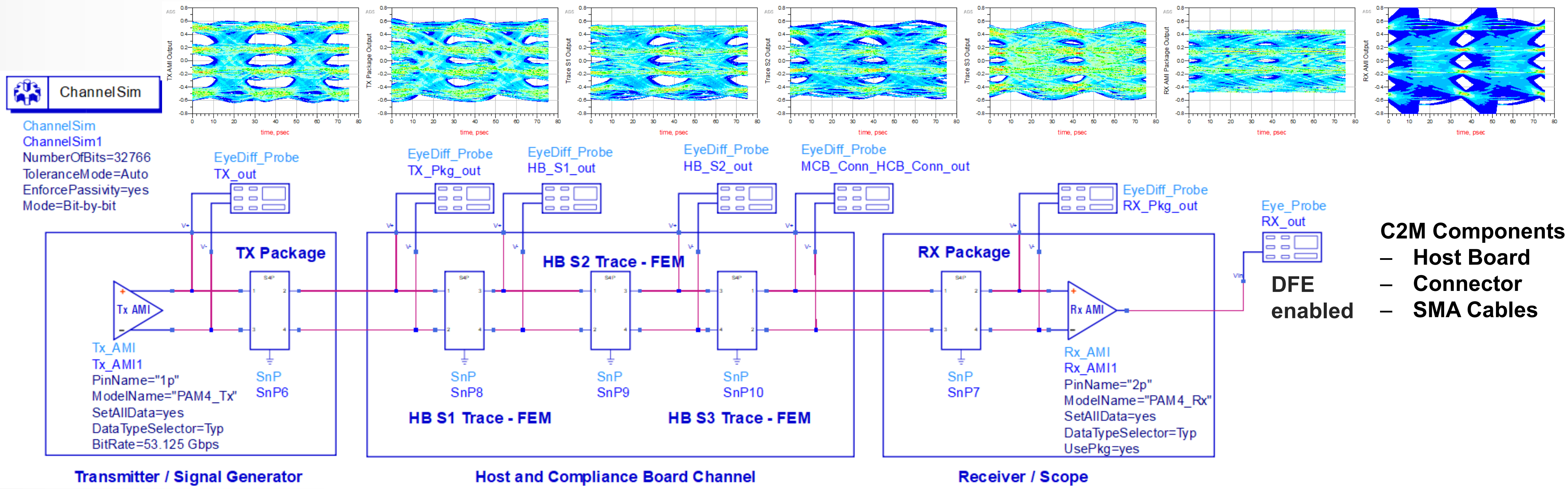
Transmitter

PAM4
From Simulation to Measurements

PAM4 Channel Simulation with AMI Model

EXAMPLE: 400G CHIP-TO-CHIP (C2C) TEST BENCH SETUP

- Keysight ADS SW provides comprehensive PAM4 Channel Simulation Analysis using vendor IBIS-AMI models
- AMI Models provided by Chip Vendors, encapsulating TX & RX performance without disclosing Chip Vendors IP
- Test Setup: TP0 to TP5 (ball-to-ball)



AMI (Algorithmic Modeling Interface)
FFE (Feed-Forward Equalizer)
IBIS (IO Buffer Info Specification)
CTLE (Continuous Time Linear Equalizer)
DFE (Differential Feedback Equalizer)

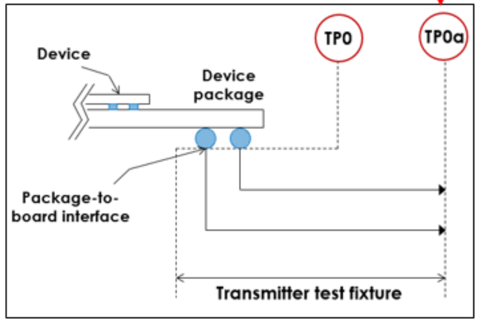
http://www.eda.org/ibis/

Correlate PAM4 Simulations with Measurement

ADS 2019 TO FLEXDCA "CONNECTED FLOW"

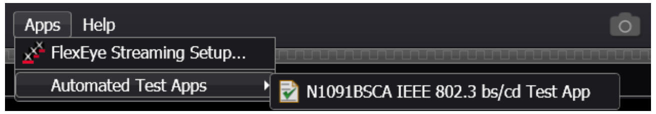
- Connects simulation and measurement domains seamlessly: **"Design to Test"**
- Uses the **same measurement algorithm** and methodology on both simulated and measured waveforms
- Expands ADS PAM4 measurement capabilities to include **Jitter analysis and TDECQ**
- Runs **compliance apps** on simulated and measured waveforms

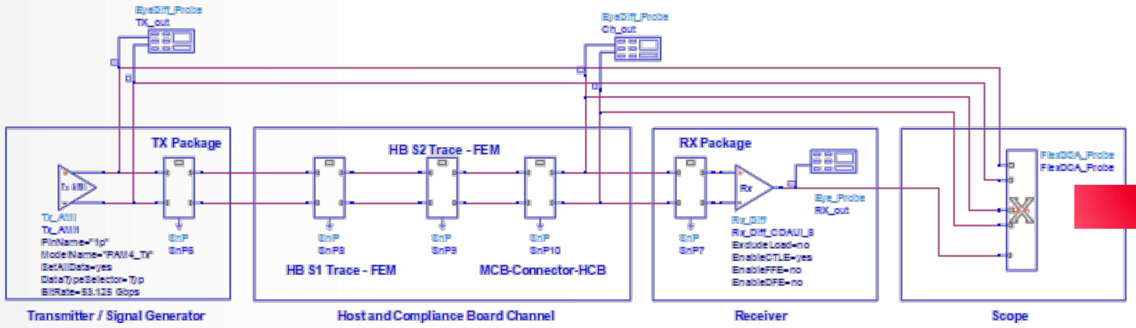
Scope goes here…

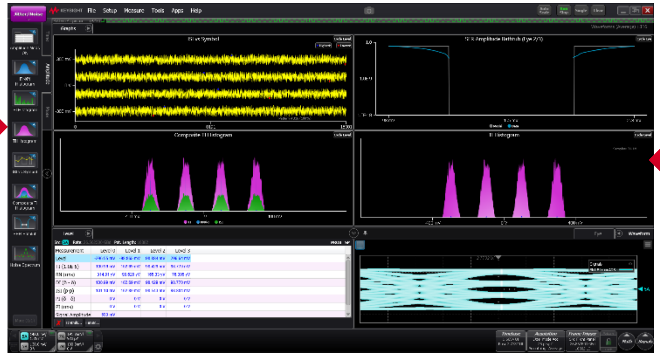


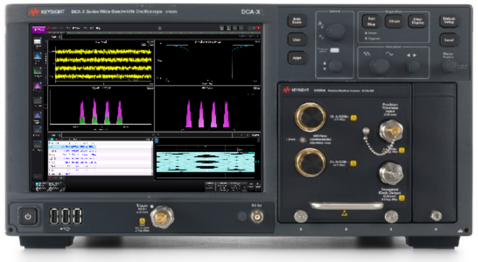
Transmitter compliance measured at TP0a

Compliance Apps









ADS
Simulation Domain

FlexDCA – Eye/Jitter Analysis

DCA-X Oscilloscope
Measurement Domain

PAM4 Device Characterization

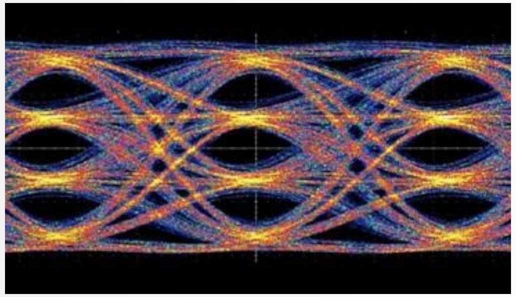
Optical Transceiver Modules Compliance Tests

400GBASE-LR8/-FR8

IEEE802.3bs Annex 120E
Chip-to-module 200 Gb/s four-lane Attachment Unit Interface (200GAUI-4 C2M) and 400 Gb/s eight-lane Attachment Unit Interface (400GAUI-8 C2M)

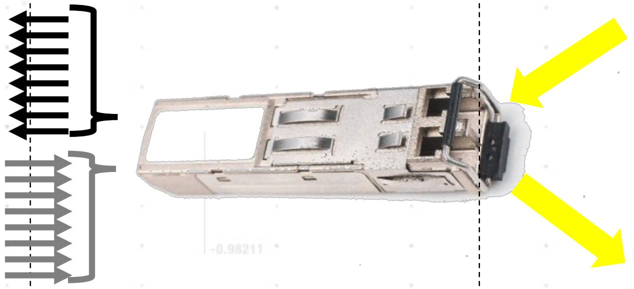
IEEE802.3bs clause 122
Physical Medium Dependent (PMD) sublayer and medium, type 200GBASE-FR4, 200GBASE-LR4, 400GBASE-FR8, and 400GBASE-LR8

26.6GBd PAM4



Electrical Tx test
Linearity, ISI, Mask
(Waveform analysis)

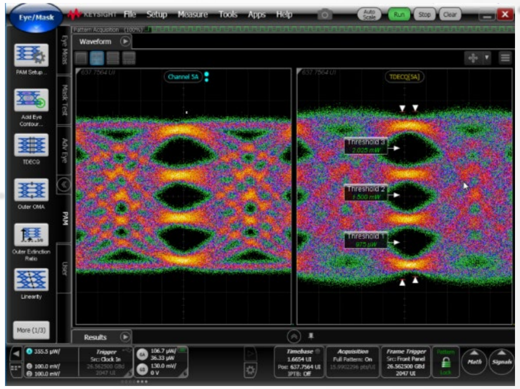
Electrical Rx test
SRS, Jtol (BER)



Optical Rx test
SRS, Jtol (BER)

Optical Tx test
TDECQ, OMA, OER
(Waveform analysis)

26.6GBd PAM4



400GAUI-8 C2M

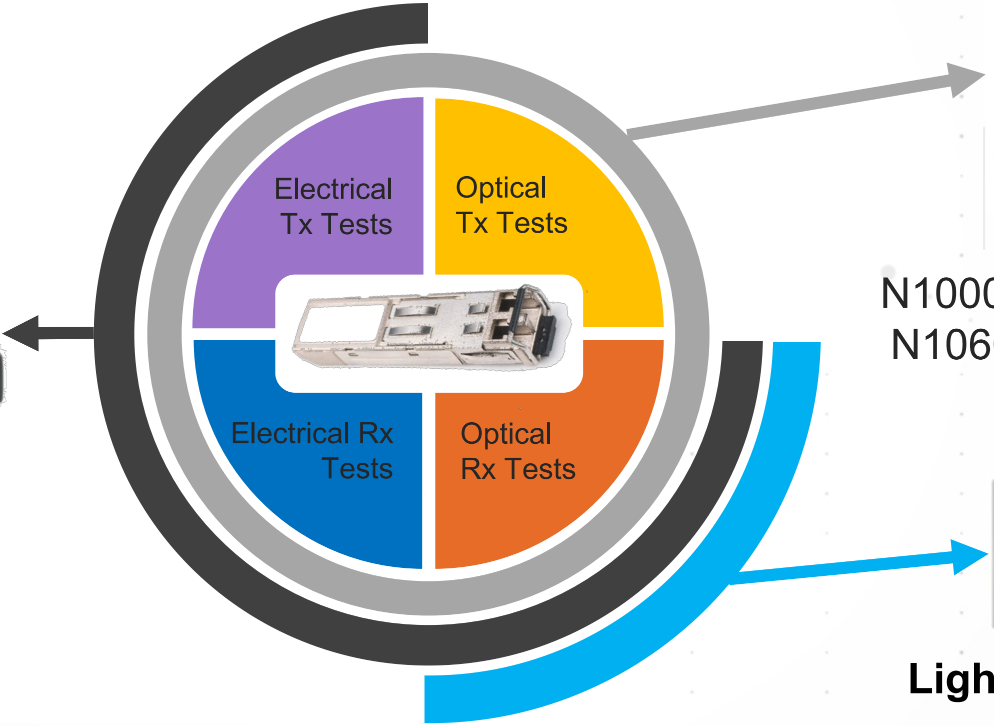
400GBASE-FR8/LR8

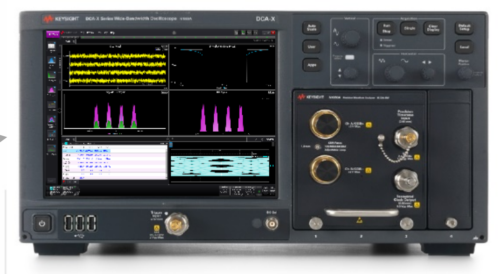
SRS - Stressed Receiver Sensitivity
Jtol – Jitter Tolerance

Optical Transceiver Modules Compliance Tests

400G SOLUTIONS FOR DIRECT DETECTION

M8040A BERT System
M8045A Pattern Generator
M8046A Analyzer Module
M8057A/B Remote Head
M8054A interference source
or M8195A/M8196A AWG





DCA-X Oscilloscope
N1000A DCA-X Sampling Oscilloscope
N1060A Precision Waveform Analyzer

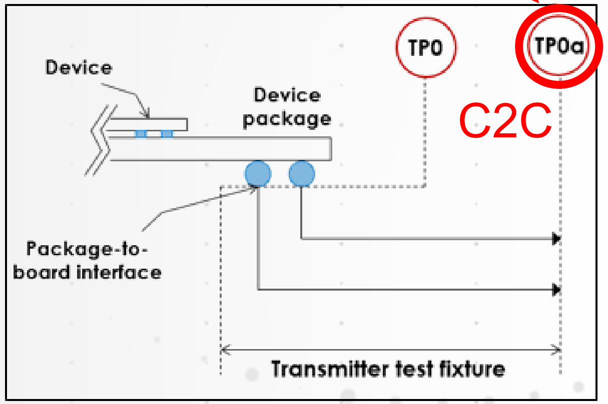
Lightwave Measurement System
8164B Mainframe
8149x optical Ref Tx
81609A Tunable Laser Source
81576A Optical Attenuator

Direct Detect Output (Transmitter) Test

Where Do the Tx Parameters Get Tested?

IEEE 802.3BS ELECTRICAL TX TEST POINTS

Scope goes here …



Transmitter compliance measured at TP0a

Chip-to-Chip (C2C) at TP0a (custom fixture)

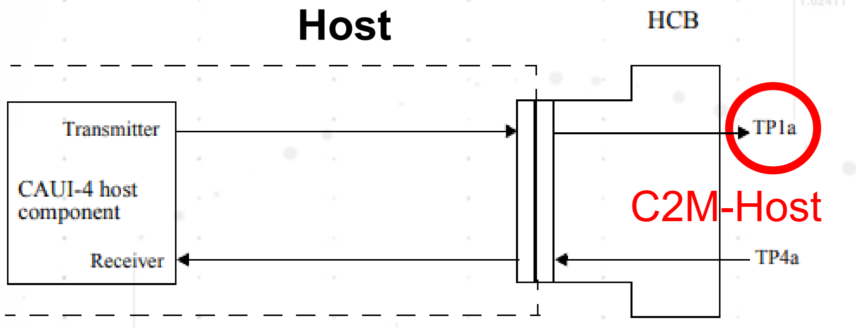


Figure 83E–4—Host CAUI-4 compliance points

Chip-To-Module (C2M) at TP1a (use compliant fixture)

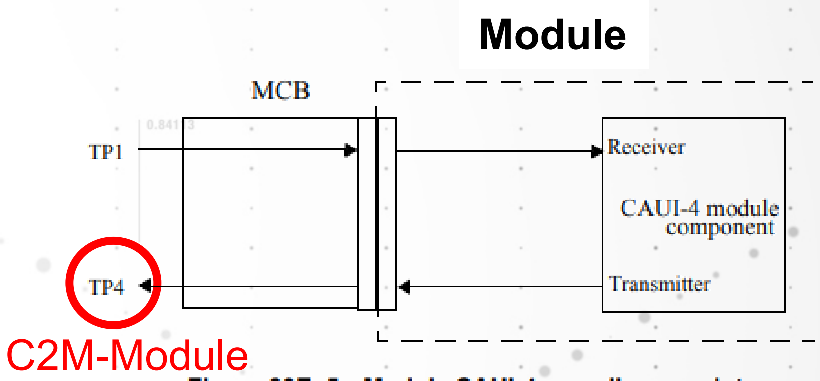


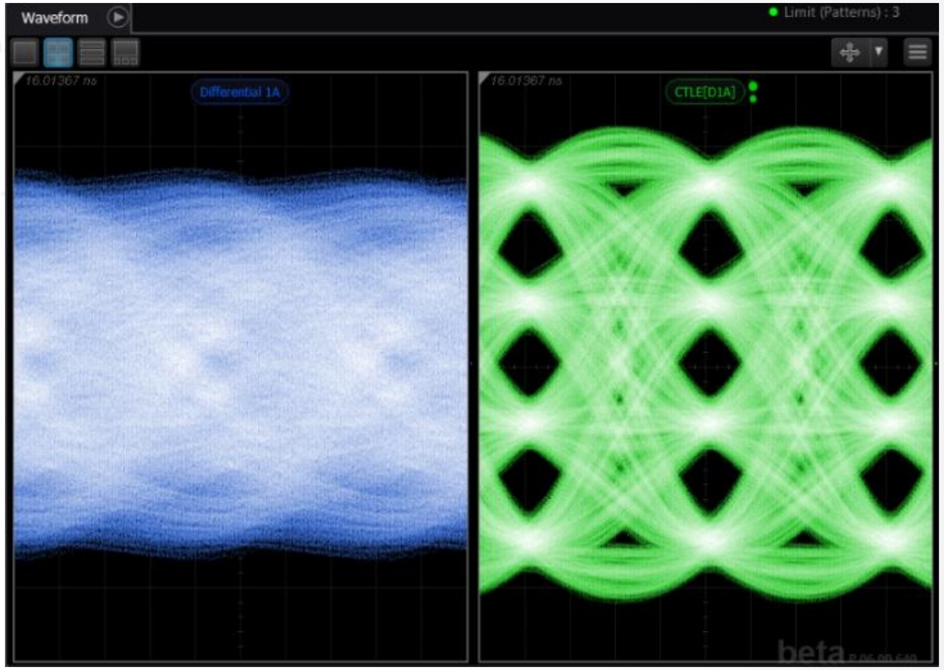
Figure 83E–5—Module CAUI-4 compliance points

Chip-to-Module Module Output (C2M) at TP4 (use compliant fixture)

Measurement Challenges for PAM4 Test

NEW ANALYSIS METHODOLOGY REQUIRED TO ANALYZE DEGRADED SIGNALS

- **Baud rates continue to increase (from 26 to 53 GBd)**
  - Standards (IEEE 802.3bs/cd, CEI 4.0,...) require:
    - ✓ higher bandwidth test equipment
    - ✓„ideal“ 4th Order Bessel-Thomson reference receiver response
    - ✓equalization to open signals for analysis
- **Degraded PAM4 Eyes with higher Baud Rates**
  - Signal-to-Noise penalty of $20 \cdot \log(^1/_3) = -9.6$ dB (vs. NRZ) making PAM4 more susceptible to noise
  - Inherent ISI in PAM4 signals reduces EW/EH margins
  - Channel loss often results in closed eyes making analysis difficult
  - Requires low noise reference receivers and advanced clock recovery
- **Complex New Measurements**
  - Requires advanced analysis tools

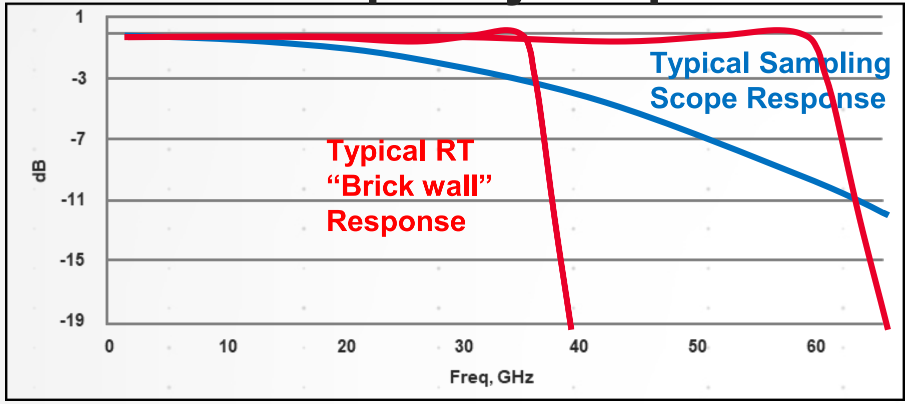


Raw signal w/o EQ

After EQ

Compliant Frequency Response (Reference Receiver)

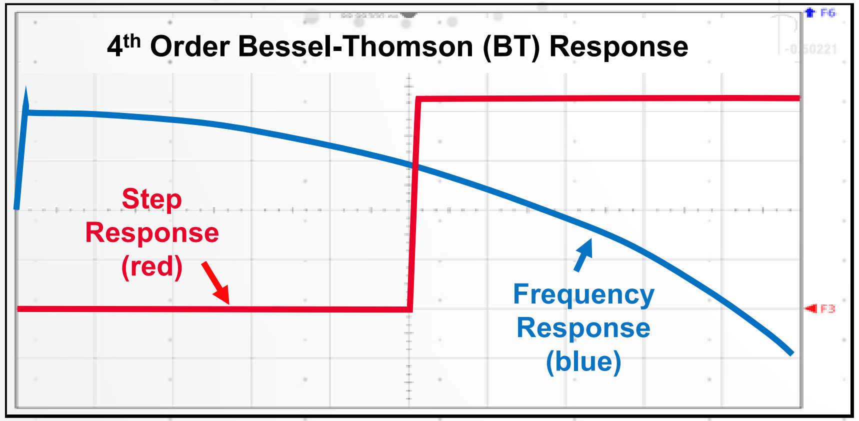
Receiver Frequency Response:



Scopes have different frequency responses:

- ➢ Will result in different eye/waveform shapes and amplitudes → different measurement results
- ➢ To achieve 33/40 GHz 4th Order BT response on a RT scope, must start with > 60 GHz "brick wall" response, BW must be adjustable

To provide more measurement consistency, most standards now specify BW and shape.



Examples (26 GBd PAM4; 53 Gb/s):

- **IEEE 802.3bs™/D3.5 (Ethernet)**

Clause 120D.3.1 200GAUI-4 or 400GAUI-8 transmitter characteristics:
"A test system with a fourth-order Bessel-Thomson low-pass response with 33 GHz 3 dB bandwidth is to be used for all transmitter signal measurements, unless otherwise specified."

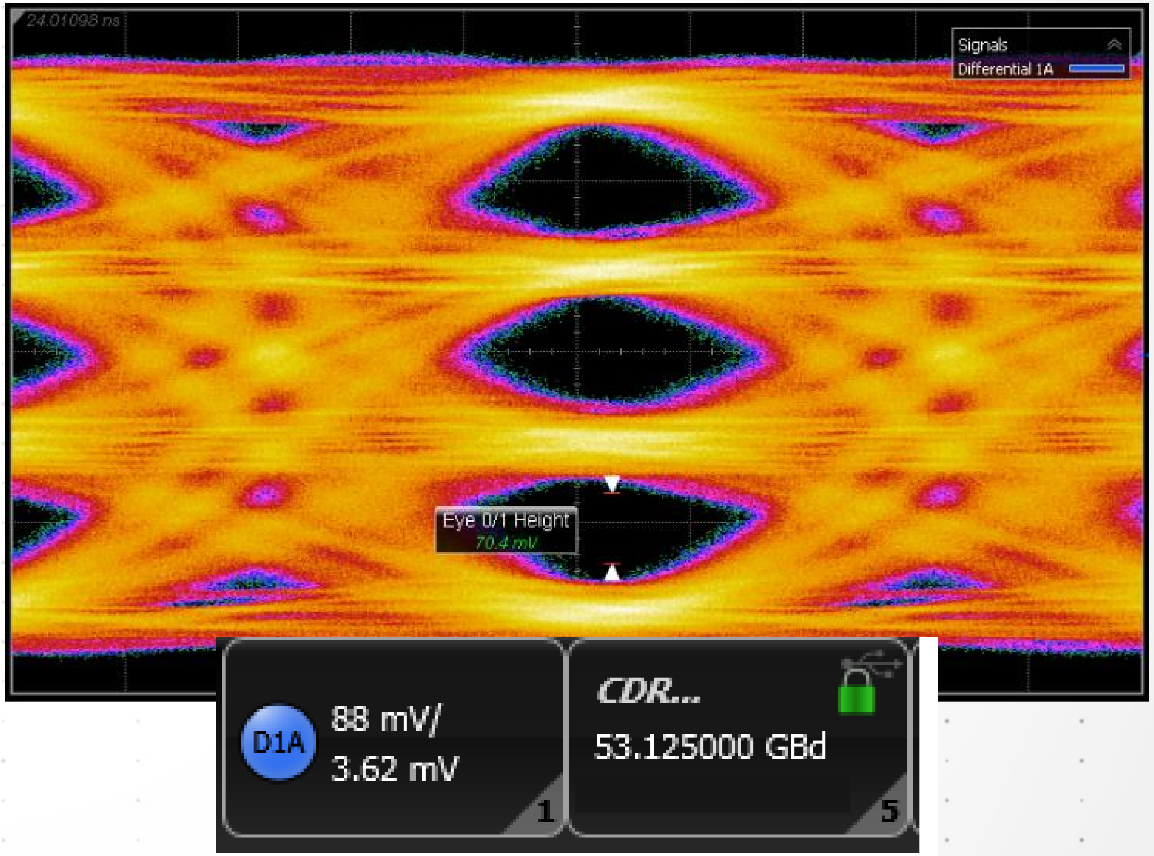
- **CEI-56G-VSR-PAM4**

Section 16.3.4 Output Differential Voltage, pk-pk
"The waveform is observed through a fourth-order Bessel-Thomson response with a 3-dB bandwidth of 40 GHz using a QPRBS13-CEI pattern."

Bandwidth for “112G” (56 GBd)

PROPOSED 43 GHZ BESSEL

- 43 GHz Bessel response is deemed to be representative of “112G” transmitters (chip -> package -> fixture)
- Will this be sufficient BW for Tx characterization? Will 43 GHz BW penalize (reduce EH/EH margins) designs with better SI performance?
- 43 GHz BW usage not finally set, may change to higher BW (>= 50 GHz)



Clock Recovery for PAM4 Designs

Clock recovery (CR)

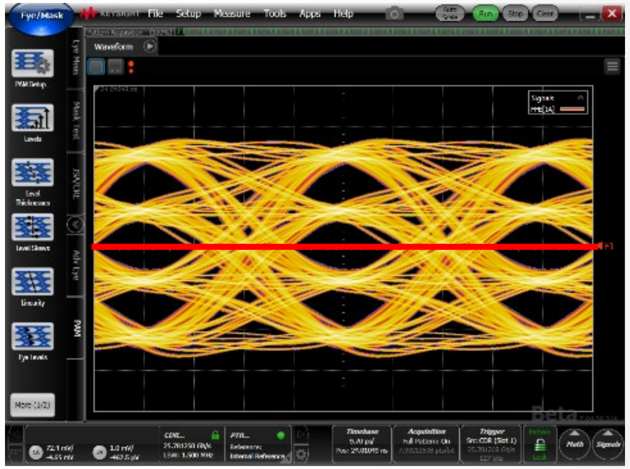
- Recovers a clock for the Rx to use in real systems
- Scopes need to emulate CR used in real Rx
  to track out low-frequency jitter, trigger the scope

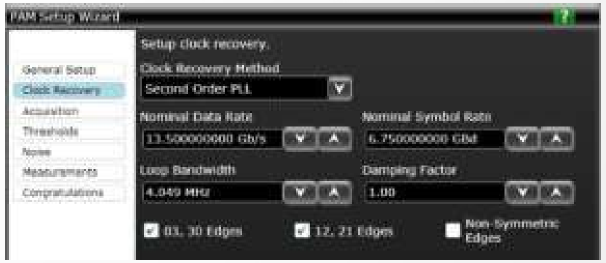
PAM4 adds complexity

- Data pattern affects transition density
- Transitions no longer only at 0V diff
- OIF-CEI proposal:
  - **1 detector: 0V crossing**
  - **allow all edges that cross to be counted**
- CR Loop BW <u>reduced</u> from 10 MHz to ~ 4 MHz
  (IEEE 802.3bs/cd and CEI-56G-PAM4, same for 112G standards)

Instrument clock recovery

- Real-time oscilloscopes use software CR
  - Transition level qualified SW CDR
    will include 0-3/3-0 and 1-2/2-1 level transitions
- Equivalent-time oscilloscopes (aka Sampling scopes) use hardware CR
  - Existing Keysight HW clock recovery designs work on PAM4 signals
- CR needs to be able to lock onto "closed eyes"

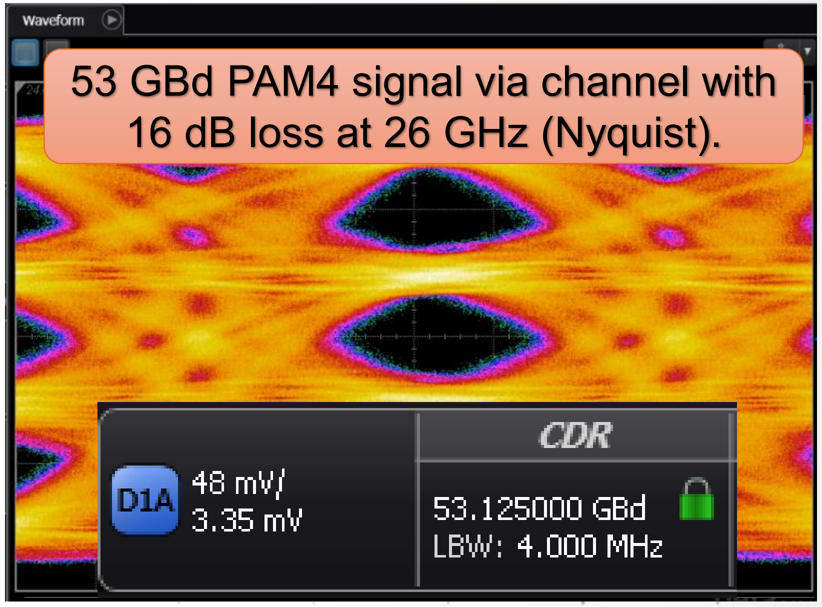




Analyzing Degraded PAM4 Signals at 53 GBd (112G)

HIGHER CHANNEL LOSS, XTALK, AND REFLECTIONS AT 53 GBD (106 GB/S)

C2M Channel Insertion Loss (IL): Up to 16 dB at 26.56 GHz (proposed). Whole link insertion loss can be more than 20 dB.

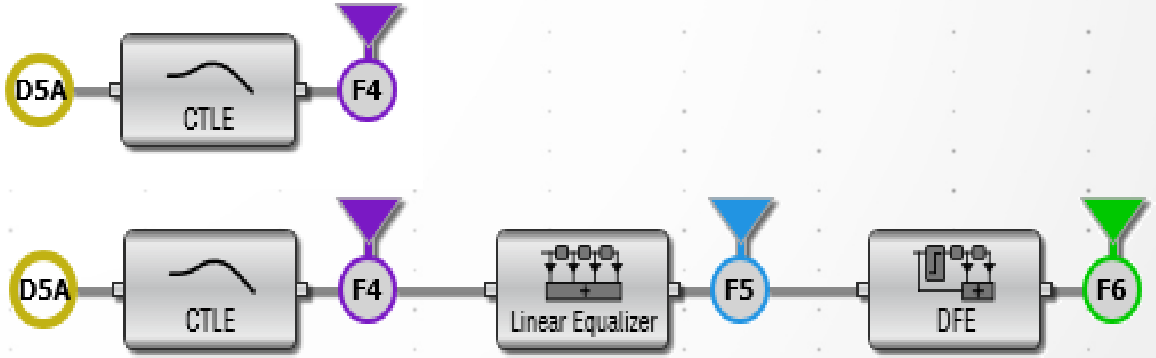


Step 1: Scope must obtain CR lock (SW or HW) in order to analyze/equalize signals

- Ensure the CR in your instrument can lock onto severely closed eyes

Step 2: Equalize the signal and analyze

- **"56G" Today:** only uses CTLE (up to 9 dB gain)
- **"112G" Future:** will likely require a combination of CTLE, FFE (5 tap?, 12 tap?), and/or DFE



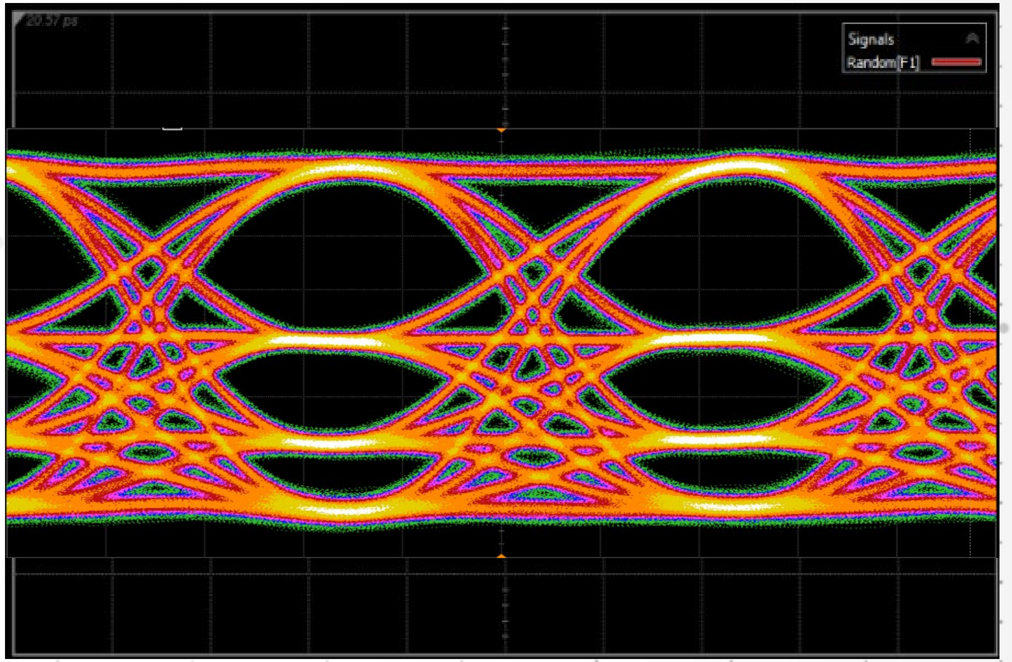
CTLE - Continuous Time Linear Equalizer
FFE - Feed Forward Equalizer, aka LFE, Linear Feedforward Equalizer
DFE - Decision Feedback Equalizer

Which Tx parameters Get Tested?

KEY PAM4 MEASUREMENTS FOR ELECTRICAL TRANSMITTERS

- **Eye Width (EW), Eye Height (EH)**
- **Eye Symmetry Mask Width (ESMW)**
- **Output waveform**
  - Level Separation Mismatch Ratio
- **Signal-to-noise-and-distortion ratio** (SNDR)
- **Output jitter**
  - J_{RMS}
  - J3u (e.g. IEEE 802.3cd)
  - J4u (e.g. IEEE 802.3bs and CEI-56G-MR/LR)
  - Even-Odd Jitter (EOJ)

While these parameters may sound familiar to you, they are measured very differently compared to legacy NRZ designs



Infiniium UXR-Series Real-Time Oscilloscope and N1000A DCA-X Oscilloscope

ENGINEERED FOR TESTING 400G/800G DESIGNS…AND BEYOND

N1000A DCA-X Equivalent-Time “Sampling” Oscilloscope
N1060A Precision Waveform Analyzer (aka “MegaModule”)

UXR-Series Real-Time Oscilloscope

Which Scope Should I Use to Characterize PAM4 Signals?

Validation / Verification — Compliance — Troubleshooting


Chip


Board Level


System

Sampling Scopes (SS), "DCA"

✓ **Best for validating/characterizing PAM4 designs**

For applications that place top priority on waveform precision:

- Highest Fidelity
  - ✓ Low noise
  - ✓ Ultra-low jitter
  - ✓ High Bandwidth
  - ✓ Highest Resolution (16 bits)
- Modular Platform
  - ✓ Electrical/Optical
  - ✓ TDR/TDT
- Lowest price for same BW
- PAM4 Analysis SW
- PAM4 Tx Test "Compliance" SW

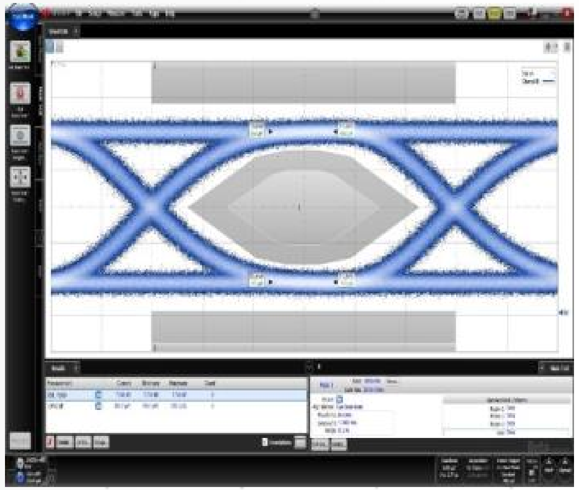
Real-Time Scopes (RT)

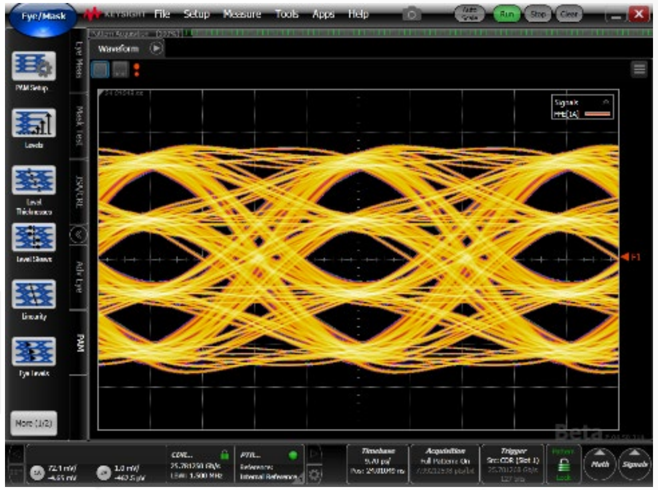
✓ **Best for troubleshooting PAM4 designs**

The most versatile tool for all areas of high-speed digital communications:

- Best for troubleshooting
- Captures one-time (glitch) events
- No explicit trigger required
- Does not require repetitive signals for pattern waveform measurements
- N7004A Optical-to-Electrical Converter
- PAM4 Analysis SW
- PAM4 Tx Test "Compliance" SW applications
- PAM4 SER/BER "Error Capture" and "Decode"

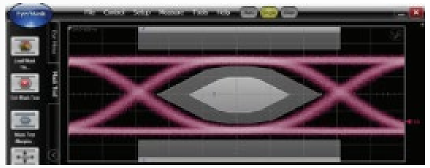
Key Measurements for Optical Direct Detection Tx

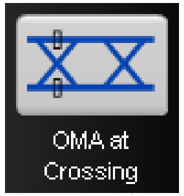


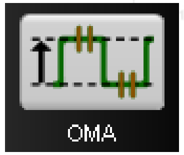


NRZ Transmitters

- **Optical Modulation Amplitude (OMA)**
  (difference between the 1 level and 0 level)
- **Extinction Ratio (ER)**
  (ratio of 1 and 0 level)
- **Transmitter Dispersion Penalty (TDP)**
- **Eye-mask**

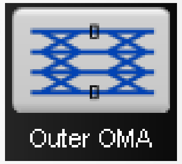


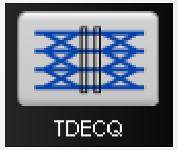




PAM4 Transmitters

- **Outer OMA**
  (difference between the 3 level and 0 level)
- **Outer ER** (ratio of 3 and 0 level)
- **Rise/fall times** (per IEEE 802.3cd)
- **<u>T</u>ransmitter and <u>D</u>ispersion <u>E</u>ye <u>C</u>losure for <u>Q</u>uaternary (PAM4) (TDECQ)**
  - ➢ Replaces mask testing!
  - ➢ Requires equalizers and "short patterns" (SSPRQ…no more PRBS31 for TX test).



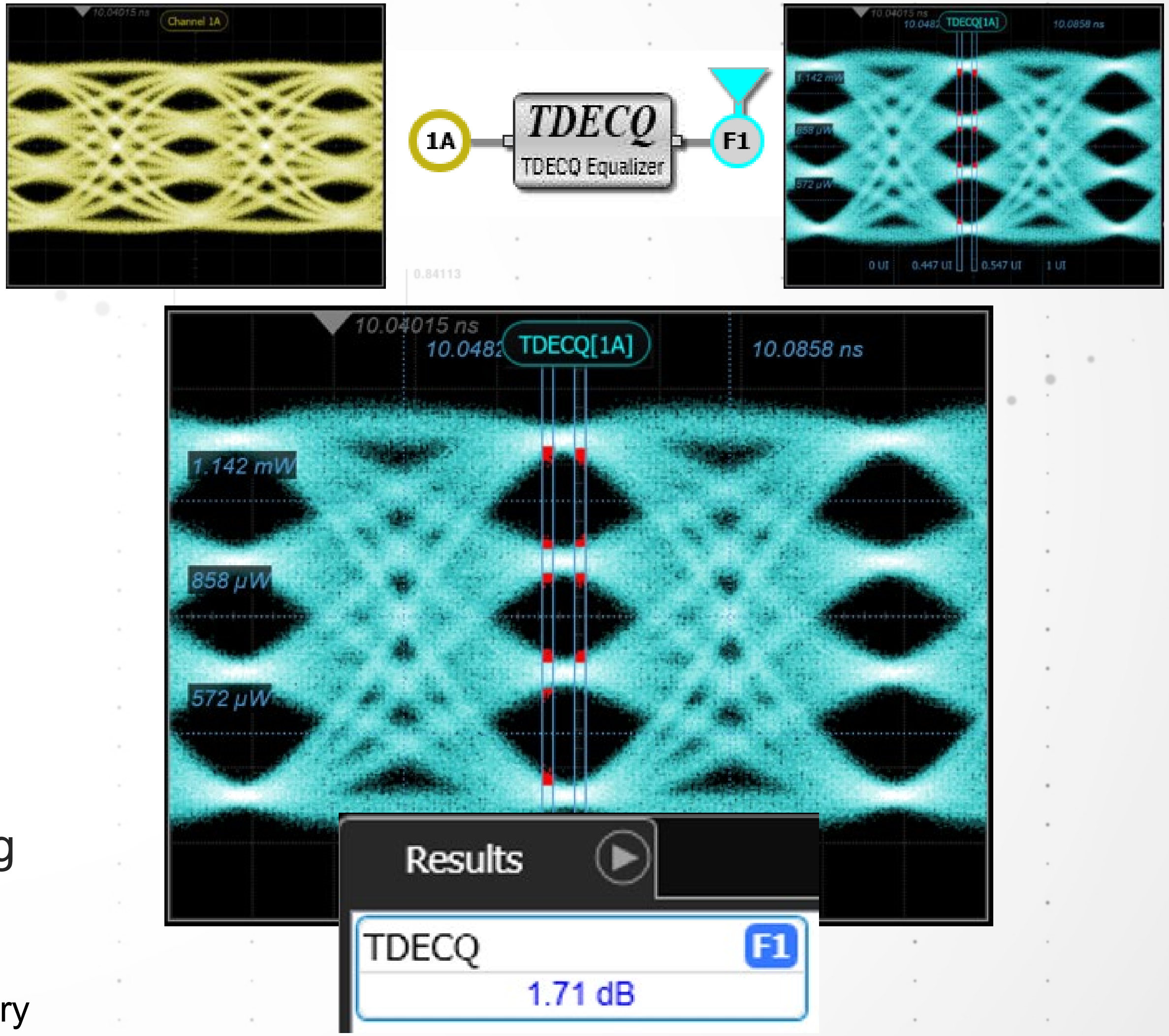


TDECQ Measurement Process

FROM IEEE 802.3BS

- Penalty against **ideal Tx** assuming a **Reference Rx**
  - Analog bandwidth of nyquist (half of actual baudrate)
  - TDECQ* equalizer: Virtual 5 tap, T spaced FFE ref. equalizer (EQ taps optimized to minimize TDECQ penalty
- SSPRQ* test pattern (2^{16}-1 length)
- Includes test fiber dispersion (single-mode)
- Oscilloscope noise measured and mathematically 'backed out'
- Histograms constructed to assess eye closure relative to OMA and compute an effective power penalty in dB for a target BER*. This is the TDECQ result. (Note: A smaller number is better)

  * 2.4 10^{-4} for IEEE 400GBase
- TDECQ <u>indirectly</u> measures SER (symbol error rate) using a scope, no BERT required



SSPRQ - <u>S</u>hort <u>S</u>tress <u>P</u>attern <u>R</u>andom <u>Q</u>uaternary
TDECQ - <u>T</u>ransmitter <u>D</u>ispersion and <u>E</u>ye <u>C</u>losure <u>Q</u>uaternary
OMA – <u>O</u>ptical <u>M</u>odulation <u>A</u>mplitude

Coherent Optical Test

Coherent Moves into the Data Center

COHERENT VS PAM4 - DATA CENTER INTERCONNECT 40-120KM

Coherent

- Higher cost
- Higher power consumption
- Higher latency (depends on DSP)
- CD compensation adaptive to link due to DSP
- In DWDM system up to 10 Tbit/s (20 Tbit/s @ 16QAM, 30 Tbit/s @ 64QAM)

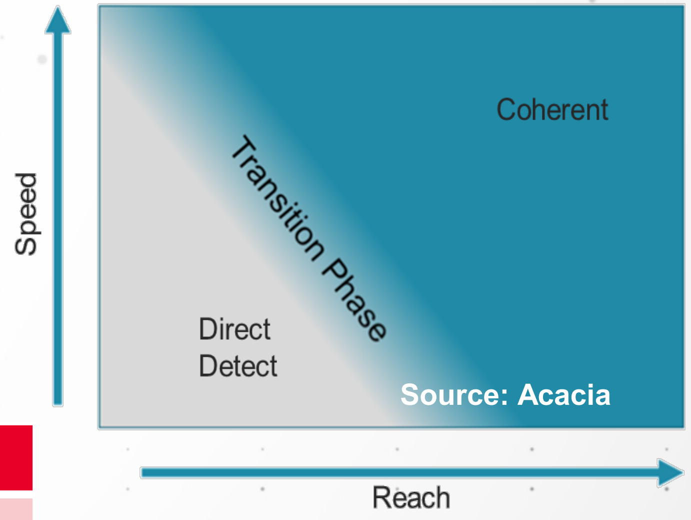
Addressed in 400ZR

PAM4

- Lower cost
- Lower power consumption
- Lower latency (but affected by CD compensation)
- Needs CD compensation depending on link length
- In DWDM system up to 4 Tbit/s
- Not true for applications that require higher speed and longer reach

DataCenter Interconnect

10 km – 40 km
6 mi – 25 mi



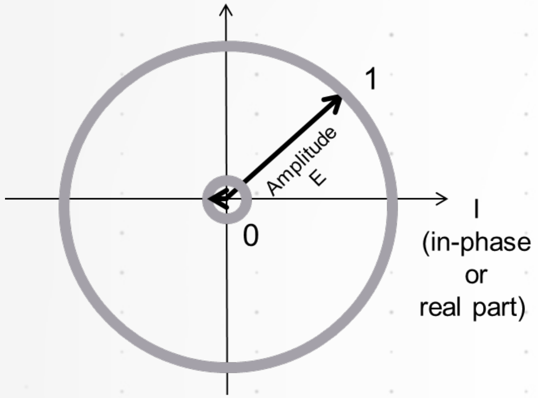
Conclusion from workshop „DSP for short-reach optics“ at OFC 2018

Speed-class	Coherent	Direct-Detection
400G (2019+)	> 10 km	< 10 km
800G (2023+)	> 2 km	< 2 km

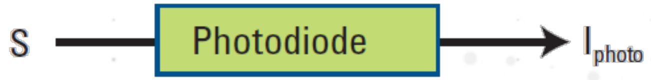
Direct Detection vs. Coherent Detection

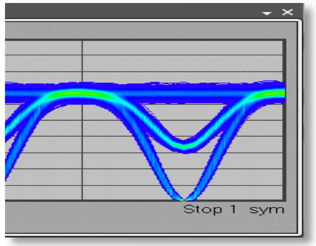
A COMPARISON OF PRINCIPLES

Direct Detection



Direct Detection Receiver
Simple Photdiode

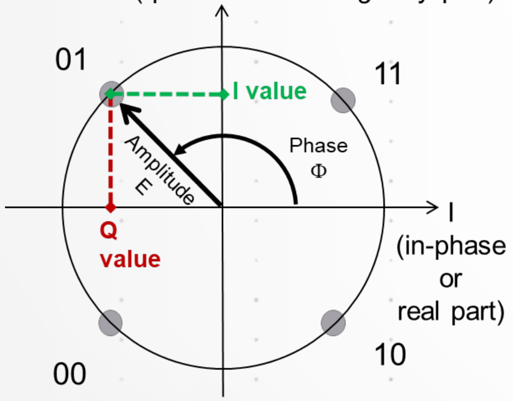




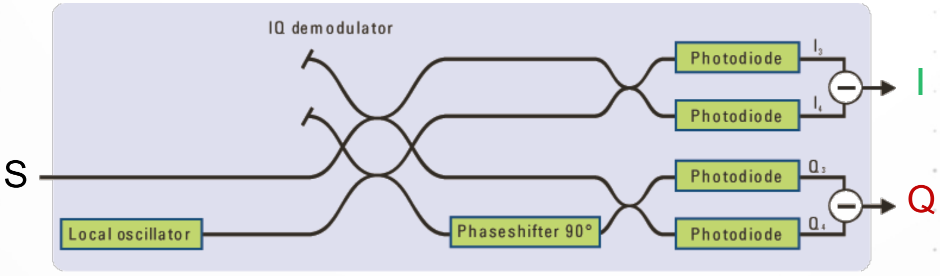
Amplitude

Information is in amplitude only
Phase can be random

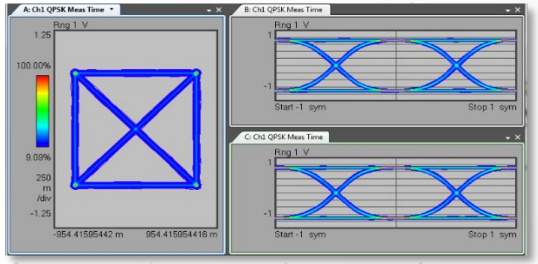
Coherent Detection



Coherent Detection
4 Photdiodes & Reference (LO)



Constellation

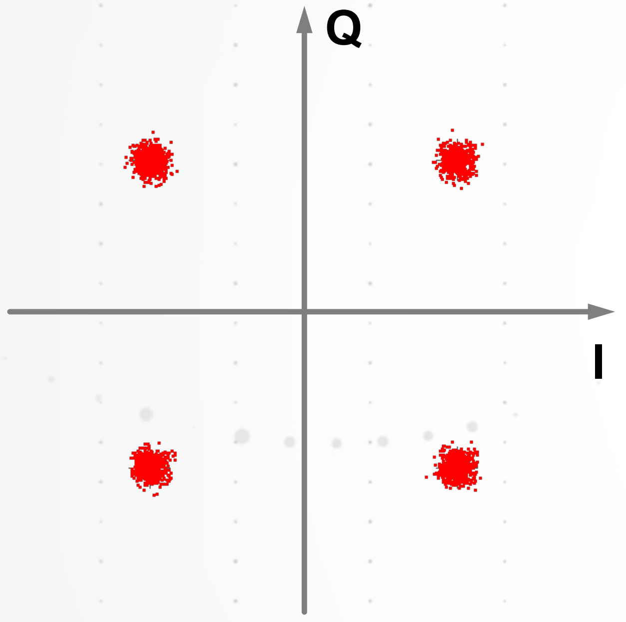


I & Q
Signals

Two balanced detectors and a reference signal allow us to have two independent measurements that contain signal amplitude and phase or I and Q

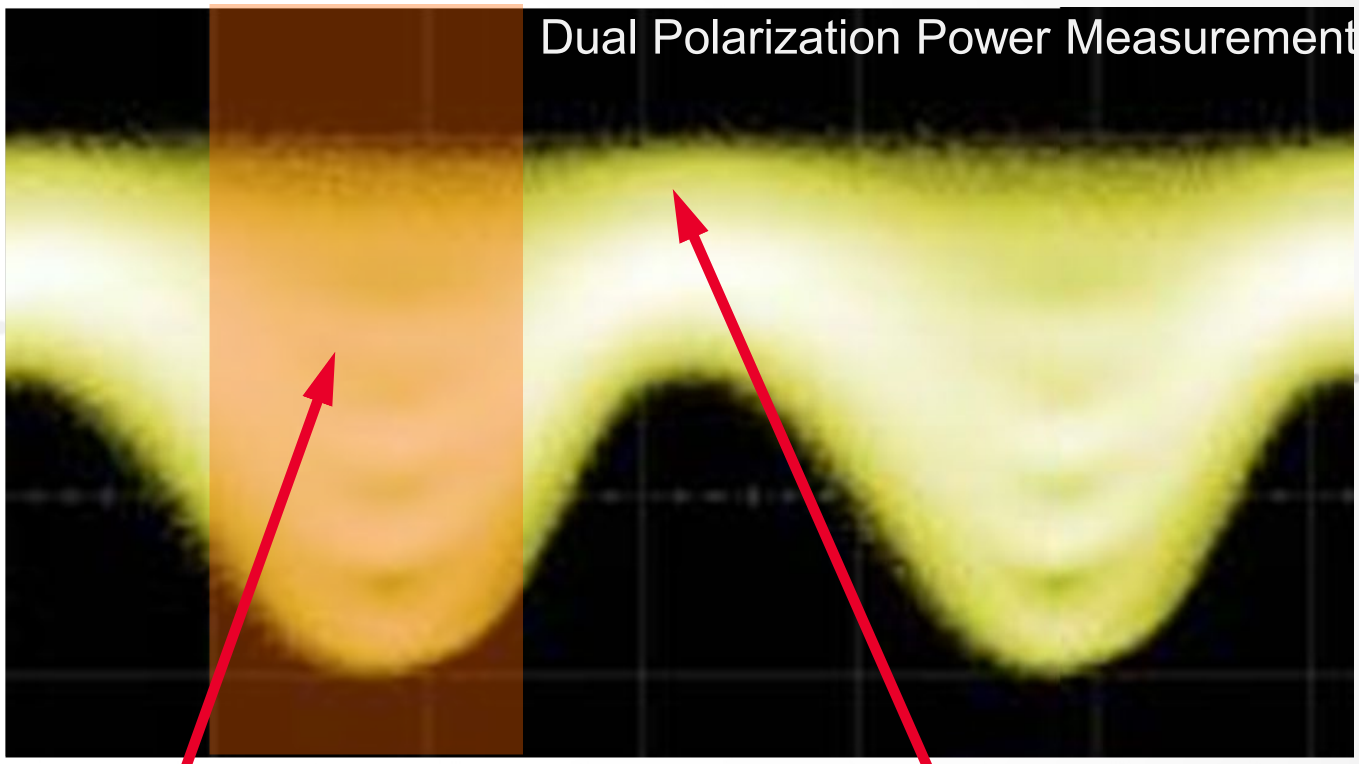
Can we analyze Complex Modulated Signals with Conventional Direct Detection Methods?

QPSK Example:



QPSK constellation map

Need amplitude AND phase sensitive measurement!



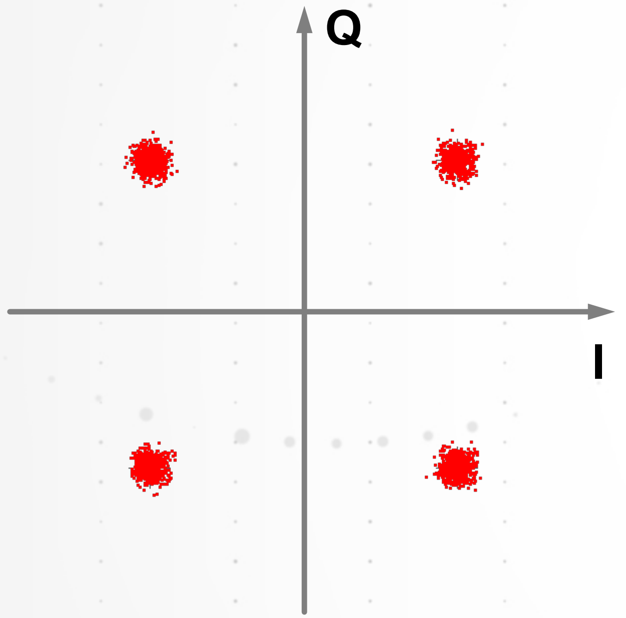
Power vs time

This is the region of transitions between symbols

This is the region where the symbol/vector state should be stable and where communications quality is assessed

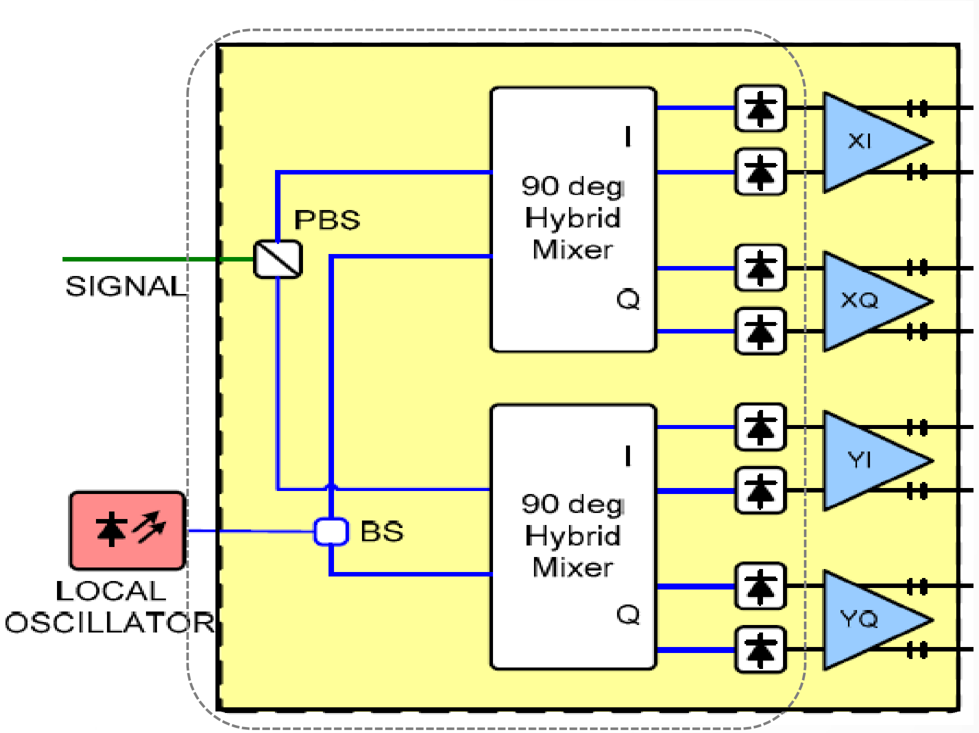
Can we analyze Complex Modulated Signals with Conventional Direct Detection Methods?

QPSK Example:



QPSK constellation map

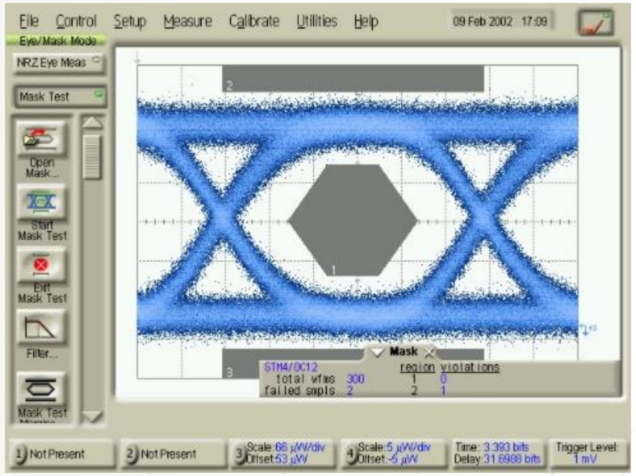
Need amplitude AND phase sensitive measurement!



Source: OIF, Document IA # OIF-DPC-RX-01.0

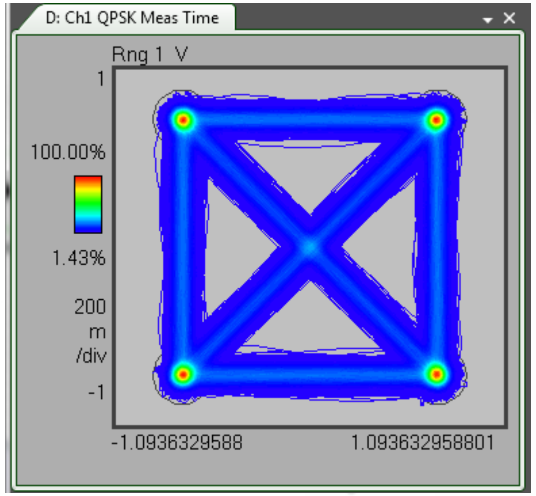
OIF implementation of a coherent optical dual polarization receiver

Different Metrics Required for Direct Detection and Coherent Transmitters



OOK (NRZ / PAM4)

- Q-factor
- Eye mask
- TDECQ
- Timing jitter
- BER
- OSNR



Complex Modulation

- EVM
- IQ Imbalance, IQ Offset
- Quadrature Error
- Frequency Offset
- BER
- OSNR

Error Vector Magnitude

QUALITY MEASURE FOR COMPLEX MODULATED DATA SIGNALS

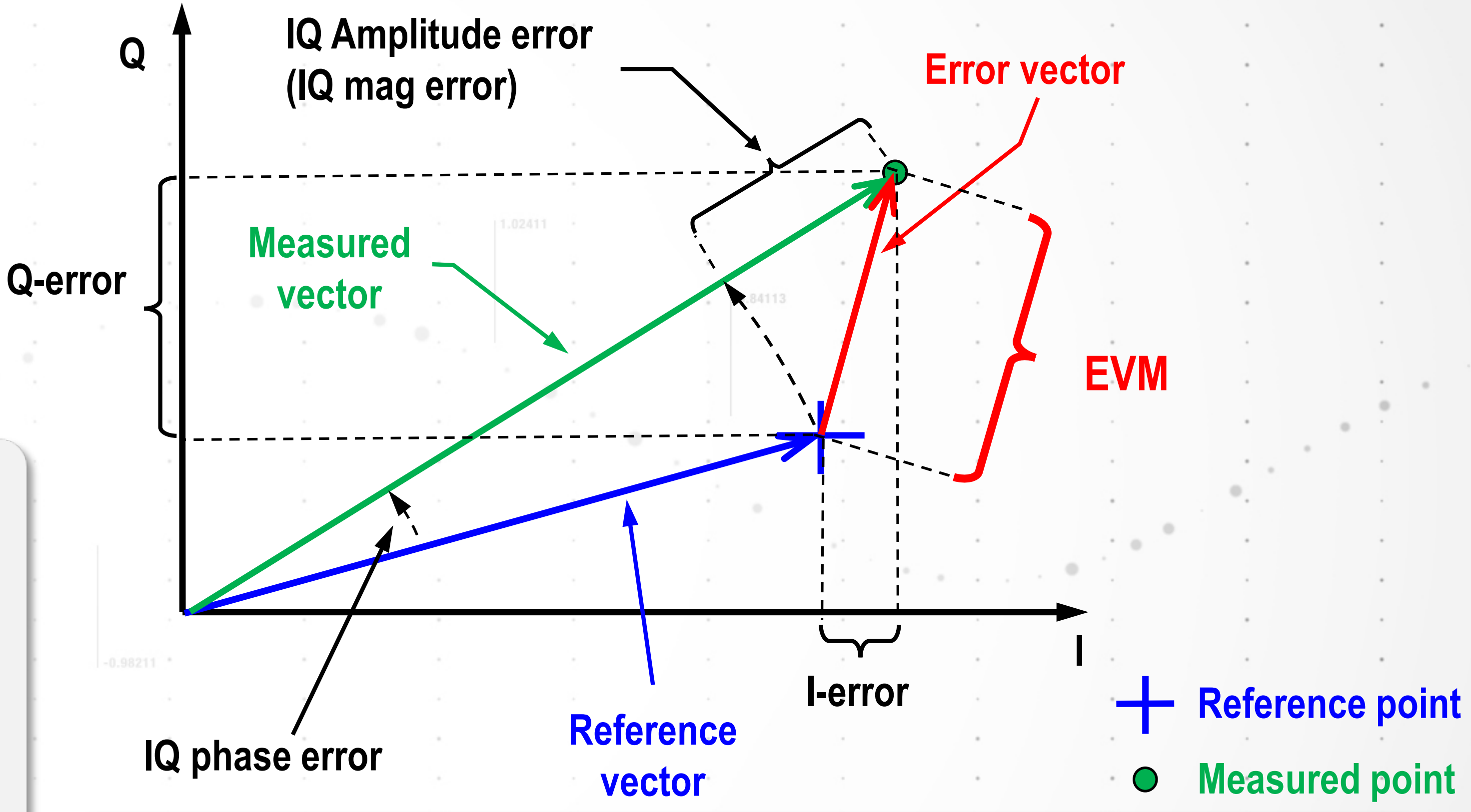
✓ Global quality metric for coherent Tx

- Needs reference receiver comprising
  - Calibrated optical front-end
  - Real-time ADC
  - Defined signal processing blocks

$$\mathrm{EVM}[k] = \sqrt{\mathrm{I}_{\mathrm{error}}[k]^2 + \mathrm{Q}_{\mathrm{error}}[k]^2}$$

$$\mathrm{EVM\%} = \frac{\sqrt{\frac{1}{N}\cdot\sum_{k=0}^{N-1}\left(\mathrm{I}_{\mathrm{error}}[k]^2 + \mathrm{Q}_{\mathrm{error}}[k]^2\right)}}{\left|\text{EVM normalization reference}\right|}\cdot 100\%$$

Where k = symbol index
N is the number of EVM points
$I_{error} = I_{Meas} - I_{Ref}$
$Q_{error} = Q_{Meas} - Q_{Ref}$

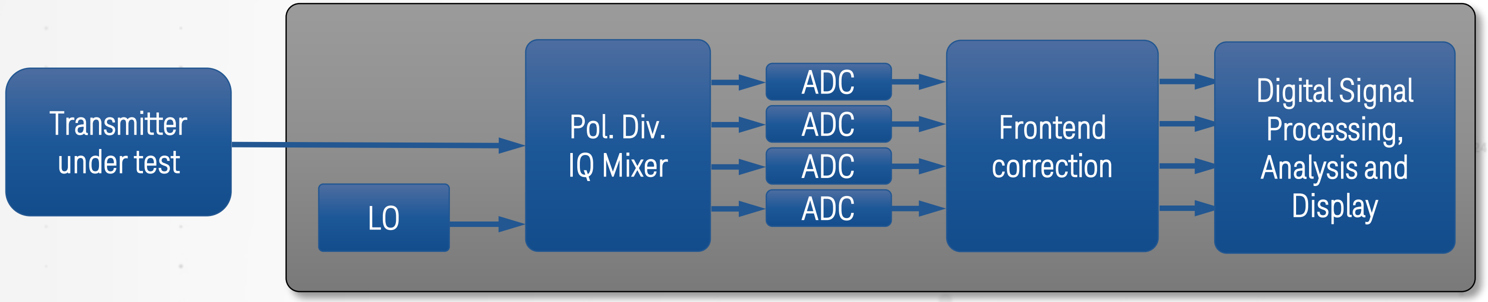


The Error Vector connects the measured vector and the reference vector!
An Error Vector = 0 means we have an ideal signal!

Method to Determine EVM

ADDITIONAL IMPAIRMENT ANALYSIS FEATURES

Proposed reference receiver



Proposed reference receiver for coherent transmitter testing:

- Dual-polarization coherent receiver
- Real-time data acquisition (four synchronized ADC channels)
- Frontend correction
- Digital signal processing

Reference receiver HW & SW characteristics need to be specified for the development of an EVM specification

M8290A modular OMA

- ✓ **Optimized for up to 400G signals**
- ✓ **Most compact**
- ✓ **Most affordable**
- ✓ **4ch. 92 GSa/s**
- ✓ **40 GHz**
- ✓ **512 kSa memory**
- ✓ **Optical Input**
- ✓ **Electrical Inputs**

Keysight supports these efforts in:

ITU OIF IEEE

Outlook

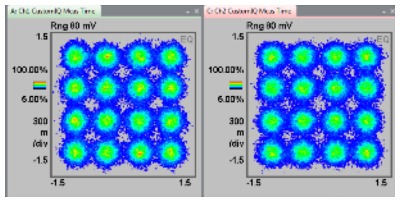
LOOKING TOWARDS 800G

- First vertically integrated non-interoperable solutions announced by Infinera and Ciena
  - Transmission rates from 100G to 800G
  - Up to 100 GBd symbol rate
  - Advanced signal processing methods like probabilistic constellation shaping and Nyquist sub-carriers
- Second generation of 800G solutions expected for 2021
  - Lower power consumption
  - Lower footprint
  - Interoperable

- The test equipment is ready

N4391B OMA
- ✓ 4ch. 256 GS/s
- ✓ 10 bit vertical resolution
- ✓ 40 – 110 GHz BW options
- ✓ 200MSa – 2 GSa memory
- ✓ Lowest noise floor
- ✓ Lowest skew

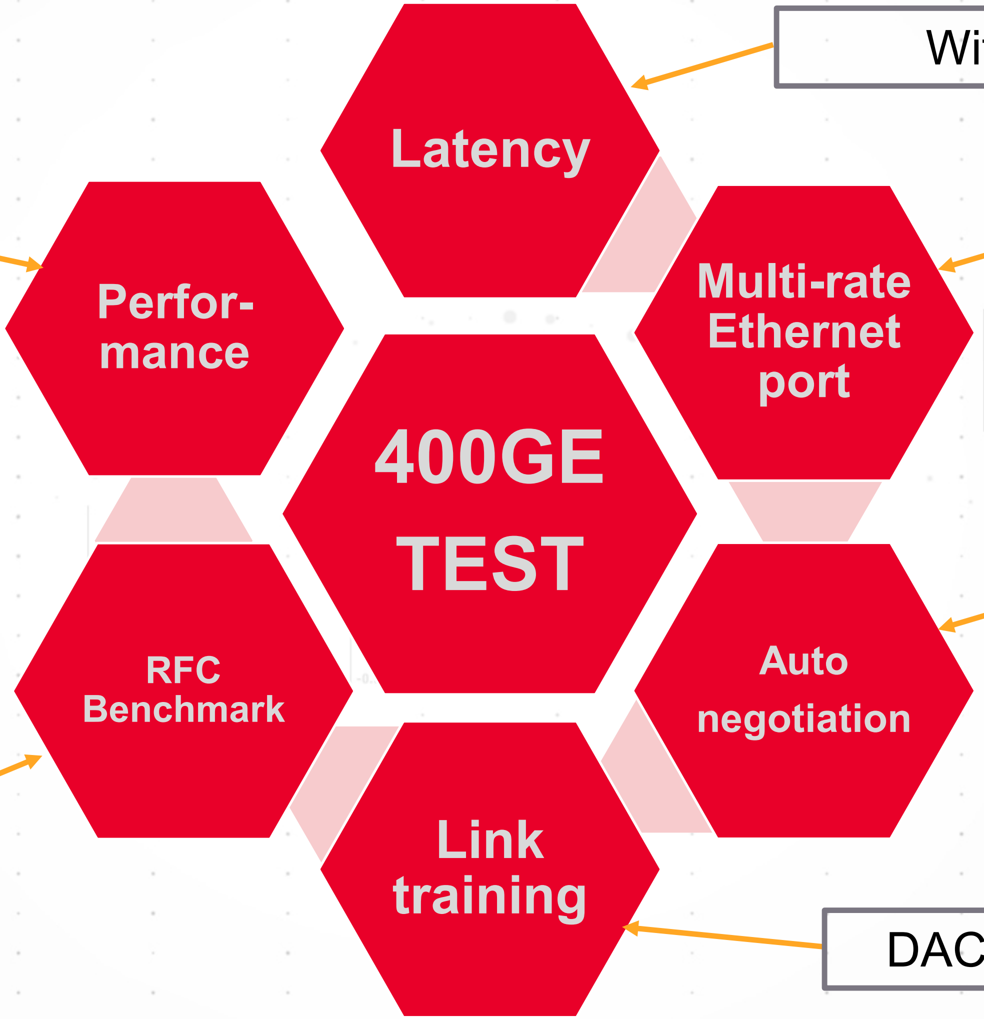
M8194A AWG
- ✓ 4ch. 120 GSa/s
- ✓ > 45 GHz 3-dB bandwidth
- ✓ Signal generation up to 50 GHz
- ✓ 512 kSa memory



DP-16 QAM constellation at **100 GBd**
Optical measurement

Layer 2-3 Test

400G (PAM4) Changes What Needs to be Tested…



With FEC

Non-blocking 100% throughput

2x200, 4x100, 8x50GE fan-outs

More interoperability

RFC 2889, RFC 2544
32x400GE +

DACs to 3-meters

FEC Analysis is Critical

400GE STD, FEC, WHAT TO LOOK FOR

- Forward Error Correction (FEC)
  - Corrects errors on the receive side (Goal: no packet errors)
  - 400G FEC corrects up to 15 symbol errors per code word
  - An uncorrectable code word results in equivalent of ~15 64B packets

CRITERIA

Pre FEC BER 10^{-4}

Frame Loss Ratio

No uncorrectable code words

HEALTHY?

Look beyond “lack of CRC errors”, pre FEC BER & FLR

Review how close to the limit of FEC

Monitor error distribution per physical lane

Monitor symbol error density

FEC Total Bit Errors	1,685,086,529
FEC Max Corrected Symbols	15
FEC Corrected Codewords	787,415,758
FEC Total Codewords	8,747,730,910
FEC Frame Loss Ratio	0.00e+000
pre FEC Bit Error Rate	3.54e-005
FEC Codeword with 0 error	7,960,315,152
FEC Codeword with 1 error	551,108,911
FEC Codeword with 2 errors	200,069,411
FEC Codeword with 3 errors	26,209,344
FEC Codeword with 4 errors	8,176,726
FEC Codeword with 5 errors	1,363,216
FEC Codeword with 6 errors	382,557
FEC Codeword with 7 errors	77,640
FEC Codeword with 8 errors	21,150
FEC Codeword with 9 errors	4,968
FEC Codeword with 10 errors	1,349
FEC Codeword with 11 errors	356
FEC Codeword with 12 errors	93
FEC Codeword with 13 errors	26
FEC Codeword with 14 errors	8
FEC Codeword with 15 errors	3
FEC Uncorrectable Codewords	0

Introducing ARESONE-400GE

3.2
Tbps

2RU
Fixed Chassis

56 Gb/s
PAM4
Encoding/
Decoding

MultiSpeed
400/200/100/
50GE

Protocol
testing

QSFP-DD
OR
OSFP

Summary

Summary - Keysight Provides Industry Leading Tools

FAST AND ACCURATE CHARACTERIZATION OF PAM4 DESIGNS

ixia
A Keysight Business

ARESONE-400GE

L2/L3 400GE Protocol Test

Modeling / Link Simulation

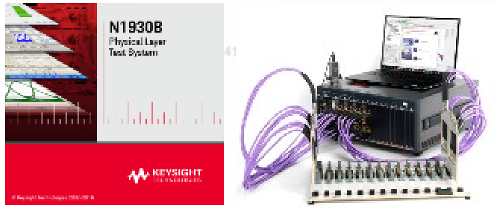
ADS, FlexDCA link

400G Design Cycle

M8040A BERT

M8194A AWG
120 GSa/s

Receiver



PLTS + M980Xa VNA

Channel/ Interconnect

UXR Real-time Scope 120

N1000A DCA-X / N1092A DCA-M Sampling Scope

Transmitter

Questions?

Please stop by the demo booth

KEYSIGHT
WORLD 2019

Acronyms

AUI = Attachment Unit Interface
C2C = Chip-to-Chip
C2M = Chip-to-Module
CDR = Clock and Data Recovery
CTLE = Continuous Time Linear Equalizer
BER = Bit Error Ratio
BUJ = Bounded Uncorrelated Jitter (used to emulate crosstalk)
DFE = Decision Feedback Equalizer
DUT = Device Under Test
EW = Eye Width
EH = Eye Height
FEC = Forward Error Correction
FFE = Feed-Forward Equalizer

NRZ = Non-Return to Zero (Refers to 2 level signaling or PAM-2)
PAM-*n* = Pulse Amplitude Modulation, where *n* = number of levels
RJ = Random Jitter
RS = Reed Solomon
SRS = Stressed Receiver Sensitivity
SER = Symbol Error Ratio
SIRC = System Impulse Response Correction
SJ = Sinusoidal Jitter
SMF/MMF = Single-mode fiber, Multimode fiber
TDP = Transmitter and Dispersion Penalty
TDEC = Transmitter and Dispersion Eye Closure
TDECQ = Transmitter and dispersion eye closure quaternary (for PAM4)